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THE DESIGN OF HIGH EFFICIENCY AND LOW POWER SWITCHED OPAMP

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Abstract

The tendency of design of integrated circuits (ICs) goes to through the power and area reduction way. The surface area of very-large scale integrated circuits is shrinking along with the shrinking of technological dimensions. Power reduction requires usage of low-power design methodologies. The design of Switched-Opamp (SwOp) circuit based on typical Operational Transconductance Amplifier (OTA), with high efficiency is presented. Reduction of power consumption, using digitally controlled switches, is provided. The suggested SwOp was fabricated in a 14nm FinFET technology and achieved a DC gain of 38.4dB, a maximum operating frequency of 11.5GHz and a power consumption of 114.48uW for worst corner (SS) when the load capacitor is 5pF. The power consumption of proposed architecture is reduced about two times. Structure proposed in the paper can be integrated in modern analog-to-digital conversion application, high-speed receivers, memory systems.

Keywords: science, Switched Opamp, typical Operational Transconductance Amplifier (OTA), operating frequency, low power, high-performance, clock gating, FinFET.

Introduction

The main parameters of modern ICs are: low power consumption and small surface area on printed circuit board. Considering their low power operation, Operational Amplifiers (OpAmps) based on MOSFETs are becoming more usable in the majority of the current electronic systems [1].

As the reference were investigated different kind of architechtures of low power OpAmps [1-2]. The disadventage of those OpAmps is that they can't be integrated in high-speed ,10MHz and more, systems. Therefore there is a need to design a new scheme of OpAmp, which will allow to increase operating frequency, in case of an acceptable increase of the power.

A typical OTA scheme based on MOSFET technology has been researched (Fig. 1) [3], which shows that all nodes, apart from the input and output ones, include either a gate-drain-connected device or a source connected to them.

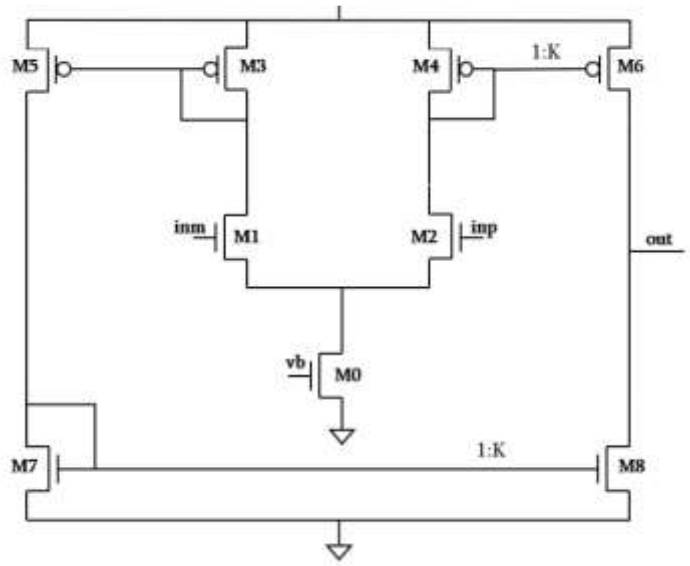

Fig 1 Typical OTA scheme

«1: K» is used to show that the width of $M6$ and $M8$ can be K (where $K > 1$) times wider than the other MOSFETs in the circuit. If it is assumed that ß1 = ß2, ß3 = ß4, so it can be observed that the current $id3$ or $id4$ is given by

$$-id3 = id4 = gm * (vp - vm)/2 = id \quad (1)$$

Moreover, if ß6 = K * ß4 = K * ß3 = K * ß5, K * ß7 = ß8,

then $id6 = -id8 = K * id4 = -K * id3$.

If the impedance of the capacitor is large compared to $ro6||ro8$, then the output voltage of the OTA is given by

$$vout = 2K * id(ro6||ro8) \quad (2)$$

and the voltage gain is given by

$$AV = vout/(vp - vm) = K * gm * (ro6||ro8) \quad (3)$$

Conflict Setting

The main problems of designing modern ICs are the reduction of the area and power consumption.

In fact, that the majority of ICs are continuously working, in order to conserve the significant amount of power, it is critical to decrease the power consumption of circuits in the IC. As a result, there is a need to do architectural changes in schemas which are widely used in very large-scale integration design and reducing power consumption in OpAmps is required nowadays. So, in OpAmps instead of reducing static power (leakage current) is preferred to reduce dynamic power by gating clock off [4-5]. And this method was used in this article while architecting SwOp design as being analog design SwOp need to use clock signal to be aligned and matched with digital circuits.

In this paper a low power SwOp using FinFET technology is designed. The design methodology of SwOp is described in next section.

Research Results

It can be seen from introduction that the maximum operating frequency of typical OTA is 155MHz, and power consumption is 217.51uW in the worst corner (Tab. 1).

Table 1

Typical OTA performance

Measurement	VDD=0.8V	VDD=0.88V	VDD=0.72V
Gain (dB)	41.6	44	22.1
Unity Gain Bandwidth (MHz)	296	529	155
Gain Bandwidth (MHz)	9.86	10.4	21.5
Phase Margin (degree)	53.8	120	11.3
Gain Margin (dB)	14.6	25.5	2.63

From the results of the research, it can be seen that in the worst case, 0.72V, a typical OTA can work at a maximum frequency of 155MHz, consuming 217.51mW of power.

Based on the designed architecture (Fig. 1) has been proposed a new circuit (Fig. 2) to improve op-amp performance and to save power consumption. [6-7]

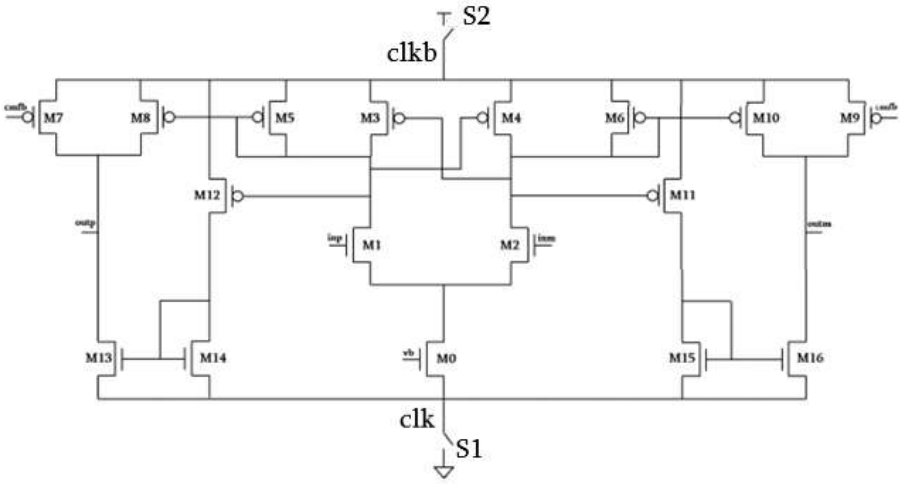

Fig 2 SwOp circuit

As it can be seen from the proposed SwOp scheme, it is based on typical OTA scheme in which was added $S1$ and $S2$ switch transistors, with help of which scheme is able to switch off the scheme from the power supply when needed and help to reduce dynamic power consumption.

Four cross-coupled transistors [7] ($M3$, $M4$, $M5$, and $M6$) are included in SwOp's load of the first stage, which brings a low impedance for common-mode signals. Thus, for different signals, that four transistors are not equal in size and the transconductance (gm) of $M3$, $M5$ ($M4$, $M6$) cannot be fully neutralized. Besides, the impedance of this node is not significantly high (about $1/(gm5 - gm3)$). Consequently, a non-dominant pole is generated by this node (Drain of $M3$ and $M5$). Also, as $1/(gm5 - gm3)$ which is much larger than $1/(ro3||ro5||ro1)$, no compensation is needed for OTA. Transistors sizes of Switched Op-amp are listed in Tab. 2.

Table 2

Transistor sizes of Switched Op-amp

Transistor	Length (um)	Number of fins	Number of fingers
M0	0.16	52	5
M1, M2	0.12	40	2
M3, M4	0.056	2	1
M5, M6	0.056	3	1
M7, M9	0.056	2	1
M8, M10	0.056	2	2
M11, M12	0.056	6	1
M13, M16	0.12	2	3
M14, M15	0.12	2	1

Common-mode feedback (CMFB) circuit allowed to keep op-amp outputs around common-mode voltage and use fully-differential topology.

The simulation results are shown in Fig. 3. Simulations are performed using HSPICE simulator [8] for 3 main PVT conditions (TT, SS and FF processes with respective voltage and temperature values). Transient analysis was run, to check the functionality of op-amp and in Fig.3 it is shown the simulation plots for TT typical corner.

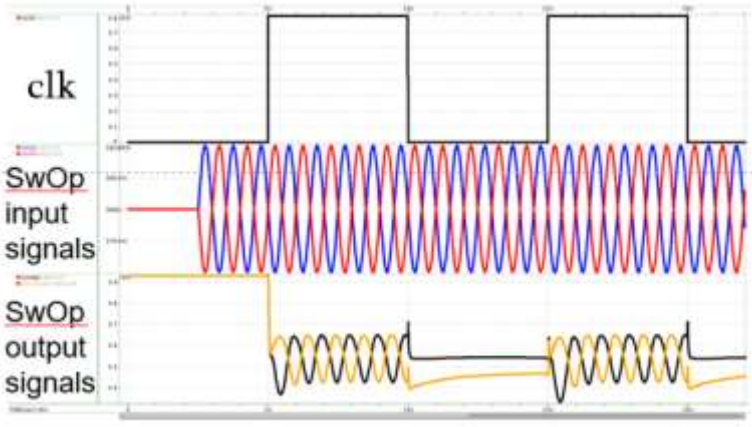

Fig. 3. Switched Op-amp transient waveforms

In the waveforms are presented clk, SwOp input and SwOp output signals. With help of positive edge of the clock signal (clk, clkb signals) SwOp is switching ON by using $S1$ and $S2$ switch transistors and amplifies input signals, and with clock signal's negative edge SwOp is switching off by saving power (Fig. 2).

SwOp simulation summary and comparison with typical OTA circuit is presented in Tab. 3.

Table 3

Comparison results of Switched Op-amp and typical OTA circuits

Process Voltage Temperature (PVT)	Measurement	Typical OTA (MOSFET)	Switched Opamp, SwOP (FinFET)
TT/0.8V/25C	Gain (dB)	41.6	49.5
	Unity Gain Bandwidth (GHz)	0.296	15.4
	Phase Margin (degree)	53.8	43.7
	Power consumption (uW)	220.52	119.2
SS/0.72V/125C	Gain (dB)	22.1	38.4
	Unity Gain Bandwidth (GHz)	0.155	11.5
	Phase Margin (degree)	11.3	34.5
	Power consumption (uW)	217.51	114.48
FF/0.88V/m40C	Gain (dB)	44	52.6
	Unity Gain Bandwidth (GHz)	0.529	19.6
	Phase Margin (degree)	120	46.9
	Power consumption (uW)	210.67	117.04

As it can be seen from the Table 3 most of the performance parameters SwOp's are better than Typical OTA's and particularly power consumption value of presented SwOp circuit to compare with typical OTA is twice lower.

Conclusion

The highly efficient high-performance SwOp architecture has been implemented in this paper. The switching operation implemented by digitally controlled switches improves the performance and reduces power consumption. The simulation results are compared with typical OTA. The disadvantage of the investigated OpAmps is that they can't be integrated with the systems with more than 1GHz operating frequency. The power consumption of proposed SwOp using digitally controlled switches, compared with typical OTA, reduced twice. In the worst corner (SS/0.72V/125C) the proposed architecture can be integrated in electronic systems with less than 10GHz operating frequency. The main disadvantage of SwOp compared with typical OTA is the large area.

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ԲԱՐՁՐ ԱՐԴՅՈՒՆԱՎԵՏՈՒԹՅԱՄԲ ԵՎ ՑԱԾՐ ԷՆԵՐԳԱՍՊԱՌՄԱՄԲ ՏԱԿՏԱՎՈՐՎՈՂ ՕՊԵՐԱՑԻՈՆ ՈՒԺԵՂԱՐԱՐԻ ՆԱԽԱԳԾՈՒՄԸ

Գ.Դ. Գրիգորյան[1], **Ա.Լ. Ալեքսանյան**[2], **Տ.Դ. Գրիգորյան**[1], **Վ.Ա. Աբրամյան**[1]

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Ինտեգրալ սխեմաների (ԻՍ) նախագծման գործընթացը միտված է էներգասպառման նվազեցմանը և զբաղեցրած մակերեսի փոքրացմանը: Գերմեծ ինտեգրալ սխեմաների մակերեսը փոքրանում է տեխնոլոգիական չափերի փոքրացմանը զուգընթաց: Էներգասպառման փոքրացումը պահանջում է ցածր էներգասպառմամբ նախագծման մեթոդների կիրառում: Հոդվածում ներկայացված է բարձր արդյունավետությամբ տակտավորվող օպերացիոն ուժեղարարի (ՕՈւ) նախագծումը՝ հիմնված տիպային փոխհաղորդականային օպերացիոն ուժեղարարի (ՓՕՈւ) վրա, որը, երկուական կոդով կառավարվող տրանզիստորների կիրառմամբ, ապահովվում է ցածր էներգասպառում: Առաջարկվող տակտավորվող ՕՈւ-ն նախագծվել է 14 նմ «FinFET» տեխնոլոգիայով և վատագույն դեպքի (SS) համար ստացվել է 38.4 դԲ ուժեղացում, 11.5 ԳՀց առավելագույն հաճախություն և 114.48 մկՎտ էներգասպառում, երբ ելքային բեռը 5 պՖ է: Առաջարկվող ճարտարապետության էներգասպառումը նվազել է շուրջ երկու անգամ: Այն կարող է օգտագործվել ժամանակակից անալոգաթվային փոխակերպիչներում, արագագործ ընդունիչներում, հիշողության համակարգերում:

Բանալի բառեր: տակտավորվող օպերացիոն ուժեղարար, տիպային փոխհաղորդականային օպերացիոն ուժեղարար, ցածր էներգասպառում, աշխատանքային հաճախականություն, բարձր արագագործություն, սինքրոազդանշանի շրջափակում, «FinFET» :

РАЗРАБОТКА СИНХРОННЫХ ОПЕРАЦИОННЫХ УСИЛИТЕЛЕЙ ВЫСОКОЙ ЭФФЕКТИВНОСТИ И НИЗКОГО ЭНЕРГОПОТРЕБЛЕНИЯ

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Процесс проектирования интегральных схем (ИС) направлен на снижение энергопотребления и уменьшение занимаемой площади. Площадь сверхбольших ИС сокращается по мере сокращение технологических размеров. Снижение энергопотребления требует применение методов проектирования с низким энергопотреблением. В статье представлена разработка высокоэффективных синхронных операционных усилителей (ОУ), основанных на типовом ОУ, который обеспечивает низкое энергопотребление с применением транзисторов, управляемых двоичным кодом. Предлагаемый синхронный ОУ проектерован по 14 нм «FinFET» технологии и в худшем случае было получено 38.4дБ усиление, 11.5 ГГц максимальной частоты и 114.48 мкВт энергопотребление, при выходной нагрузке 5 пФ. Энергопотребление предлагаемой архитектуры уменьшилось примерно в два раза. Его можно интегрировать в современные приложения аналого-цифрового преобразования, высокоскоростные приемники, системы памяти.

Ключевые слова: синхронный ОУ,типовой ОУ, низкое энергопотребление, рабочая частота, высокоскоростной, стробирования синхросигнала, «FinFET».

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