UDC - 621.383.13

DATA AND POWER SUPPLY MONITORING AND SWITCHING SYSTEM FOR IMPROVED POWER EFFICIENCY AND SIGNAL INTEGRITY

H.H. Sahakyan, R.M. Soghomonyan, D.Kh. Gabrielyan, G.A. Voskanyan
National Polytechnic University of Armenia

Power efficiency and signal integrity are one of the key performance metrics in modern communication interface design. We suggest a modern approach of improving power efficiency and signal integrity via implementing data driven supply monitoring and switching scheme. Instead of the traditional approach of having multiple slave devices in idle state waiting for the signal from the master device, the suggested solution offers a more power efficient approach of switching these devices only in case when they are in communication. The suggested architecture takes advantage of differential data line communication protocols to generate an artificial low capacity supply voltage to power small logic blocks which perform switching of supply voltages. The system also employs a non-conventional power-on-reset block to monitor the supply level. The artificial supply generating block can also be used to improve the signal integrity in open-drain/open-collector communication protocols such as I^2C, SCSI-1, etc. via verifying the authenticity of ESD events in power off devices thus preventing unnecessary current drainage. The circuit was designed and simulated using 14nm finFET technological process developed by Synopsys Armenia Educational Department. Synopsys's Custom Compiler and HSPICE were used for graphical design of circuit and simulation respectively. The circuit was tested in three extreme corners to ensure stable operation in various conditions. The results are displayed through Custom WaveView.

Key words: integrated circuit, power-efficiency, data divider, supply control, power on reset, electrostatic discharge.

Introduction

During the last thirty years, the sizes of the transistors used in integrated circuit (IC) design have shrunk enormously: from several hundred micrometers to as small as 5 nanometers [1]. This trend of decreasing the device sizes almost every year was needed because of ever increasing demands of faster and less energy consuming architectures. As the power consumption of a digital circuit is proportional to the cube of the supply voltage, reduction of the supply voltage even by a small amount has a noticeable impact on the consumed power. The less energy the circuit demands the longer the supplying battery can last. This concern is especially crucial for smaller devices with little PCB real estate to spare. Decreasing power dissipation also positively affects the longevity of the system, as devices will operate under smaller stress conditions because of lowered voltages, smaller currents and less heat. Improving power efficiency and longevity of integrated circuits can prove high profit for systems developed for commercial usage and can be a crucial improvement for systems used for biomedical applications. Another important performance metric is signal integrity which is a set of measures of the quality of the electrical signal. As digital signals are fundamentally analog in nature, they are subject to effects such as noise, distortion and loss. In some protocols, particularly ones using open-drain architecture, turning idle devices off is not a viable option as it leaves room for potential negative effects on signal integrity. One of such effects is a data signal triggering a false electrostatic discharge event which opens the clamp transistor draining a large amount of current from data line, thus dissipating more power and increasing the rise time and ring-back voltage of the signal. In some cases, the steady state value might not even reach the intended level.

Conflict setting

Digital circuits are primarily used for information processing and transmission. There are several connected devices and each one implements some functionality in a system. It may be the case

that some of the devices are not needed for some time. If the power supply can be "detached" from them then the power consumption of the whole system can be optimized. This method can be especially beneficial for slower systems where settling related delays won't be a significant sacrifice in achieving better efficiency.

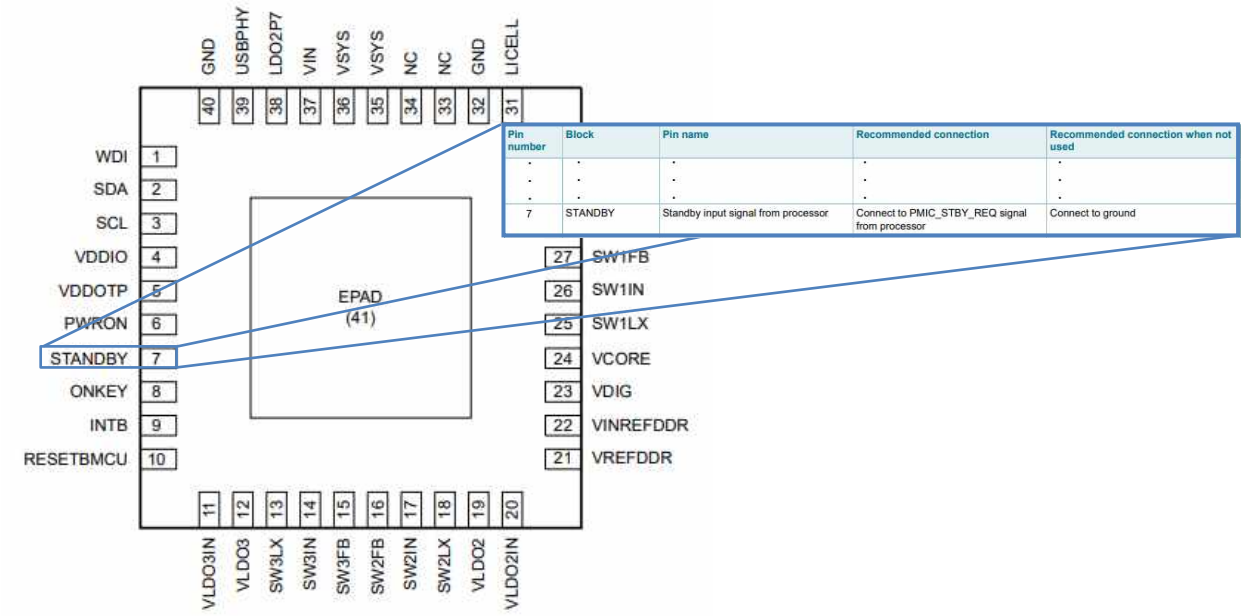

Fig. 1 PF1510 PMIC with a stand-by input pin

Most ICs have a separate stand-by input pin for controlling the power mode of the IC. Figure 1 shows such case from [7]. Some architectures like the one shown in Fig. 2 and do not require a stand-by pin, but instead use timing for detecting the stand-by input which requires a finite state machine (FSM) structure for monitoring which increases power consumption and surface area. This solution also constantly dissipates power [8].

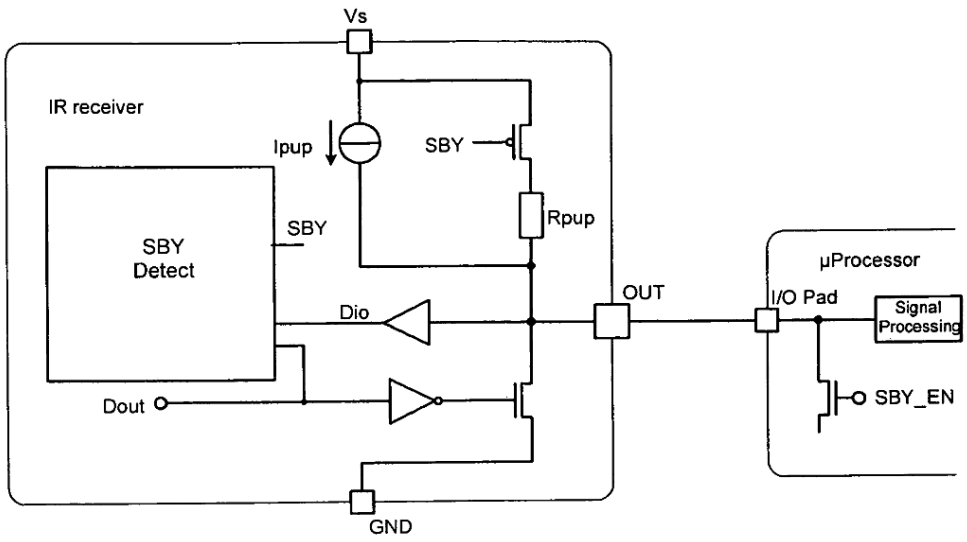

Fig. 2 Stand-by control through timing monitoring

The suggested method uses data lines to turn on or off the circuit. It takes advantage of differential data lines and requires neither constant power supply nor an external control signal. Instead it uses the signals on differential data lines as both inputs and supply. This alleviates the need of an external stand-by control and offers a monitoring system which doesn't constantly dissipate power. The block diagram of the suggested architecture is presented below (Figure 3).

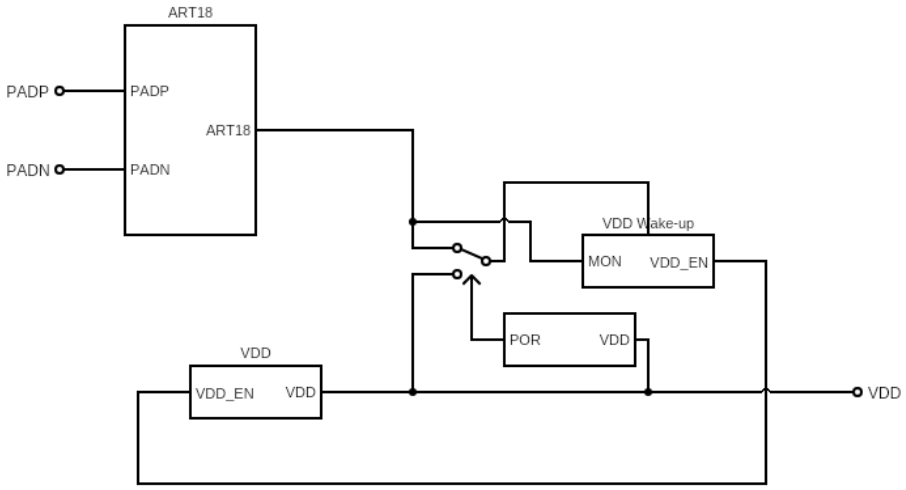

Fig. 3 Block diagram of the proposed architecture

Of course, attaching and detaching the power supply from these unnecessary devices can only be achieved through another system that decides and performs the switching. This means that there must be some other and presumably smaller system constantly monitoring which devices do not need power for the given time. This solution can be easily implemented but it requires a precise definition for what it means "a subsystem does not need to be connected to the supply now". A much easier way to solve the issue is to embed this monitoring into the system itself. A sub-circuit can be "activated" only when it has inputs to process. This means that the data itself can be the trigger to activate or deactivate the power source.

ART18 data divider is a block with two inputs and one output. The inputs are the lines of differential data and the output is a voltage equal to VDD. The VDD block is the main supply itself. The VDD wake up block is a logic circuit that detects the presence of data and turns the VDD supply on or off. It is supplied by either the 3v3 data divider block or from VDD and the latter case is when the VDD is turned on. The structure of each individual block will be presented next.

The ART18 block is a voltage divider with diode connected transistors in series. The scheme is presented in Figure 4.

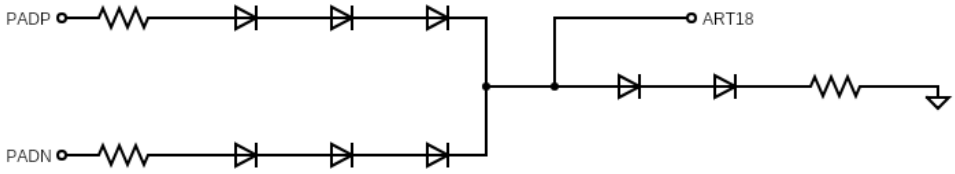

Fig. 4 ART18 data divider structure

PADP and PADN are the differential data inputs and art18 is the output of the circuit. When there is no data being transferred through data lines both PADP and PADN are 0. However, when data is transferred either PADN or PADP will be 3.3V. The ART18 output will be generated by dropping 3.3V down to about 1.8V through diode connected transistors. The circuit is enabled or disabled by means of two transistors, M1 and M3 which receive a digital signal on their gates that indicates whether the supply voltage has reached some predefined level or not. After the VDD supply passes the Power-on-Reset (POR) threshold value, the circuit is disabled and the VDD Wake-up logic, powered by VDD directly, continues to monitor PADP and PADN. When they both become 0 VDD Wake-up turns VDD off and switches its supply to ART18.

The previous discussion implied the existence of a VDD detection circuit. Figure 5 shows this supply detecting POR circuit [2].

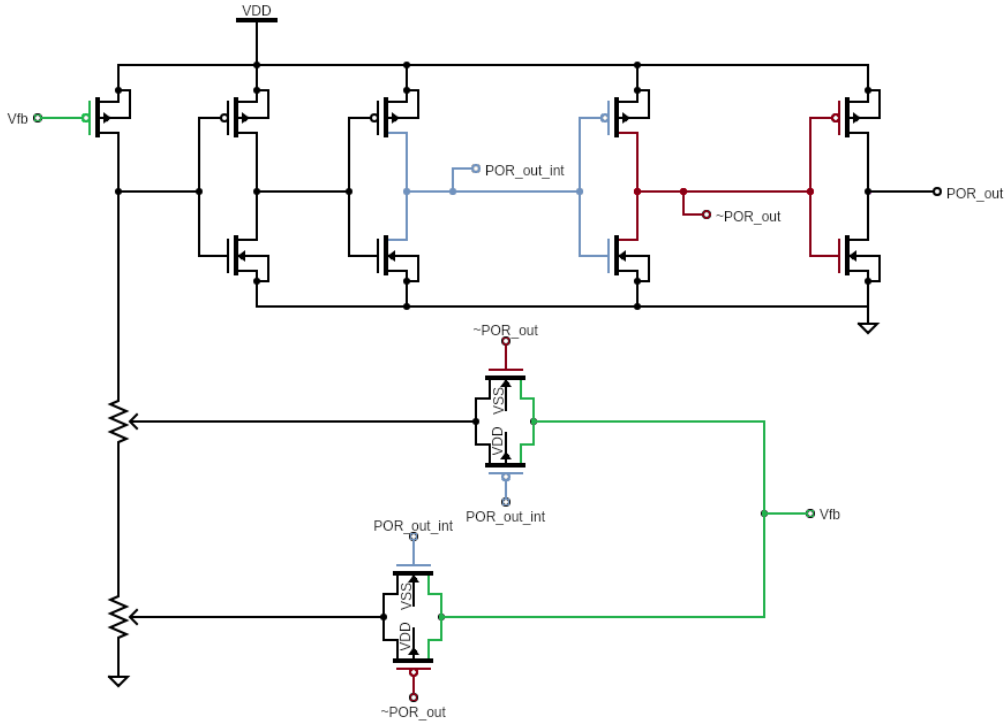

Fig. 5 VDD detection POR circuit

The two pass gates are used to define two different threshold voltages for the circuit. When VDD is zero, the circuit outputs zero, as the input of the first inverter is low (by means of resistive pulldown [3]) and it also outputs VDD which is low. This is true for all the inverters in the chain. When the VDD rises from zero, it must pass through the higher threshold defined by the pass gate which receives its input on the gate of PMOS from the POR_out_int net. When VDD passes this threshold value, the output of the circuit starts following VDD and the pass gate which was on, turns off and the other one turns on and the threshold value changes. When VDD falls from its nominal value towards zero, the reverse of the actions described in the previous case take place, differing only in the threshold value. The simulation results for this circuit will be presented in the next section.

The purpose of VDD Wake-Up block is to turn VDD on when differential data is present on the inputs and turn it off in opposite case. The exact procedure won't be described in this paper as it is a defined implementation and can be synthesized depending on the given structure.

Figure 6 shows cases of another application for artificial supply voltage block that solves previously mentioned false ESD event detection issue in open-drain communication standard [4], [5].

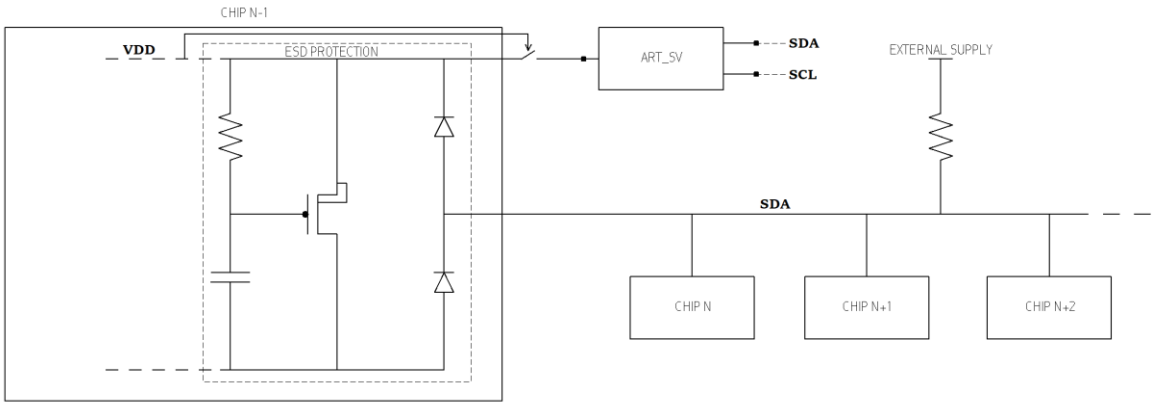

Fig. 6 False ESD detection prevention architecture

When VDD is off, the switch toggles on and ART_SV block is connected to ESD protection circuit. After a small amount of time the artificial SV stabilizes and provides the ESD diode a strong reverse bias. Now a much higher voltage is required at the anode of the diode to turn it on. Note that this implementation assumes that when the device is off, its elements are properly pulled up and pulled down to prevent any static current flow through the circuit. If this is not the case, then a more complex switching system will be required.

As any IC has ESD protection on its pins, when it gets powered off, the issue of static current drainage through the ESD diodes cannot be overlooked and it is solved by having a constant bias on the powered off supply rail. Any solution that suggests turning off idle devices on open-drain communication but ignores the possible ESD event detection is incomplete. While some power might be saved by turning the devices off, the false ESD events will not only add to power consumption but also jeopardize the integrity of communication.

Research results

The circuits were simulated using SAED 14nm [6] technology with HSPICE circuit simulation program. The simulations were done for three PVT (process, voltage, temperature) corner variations shown in

Table 1

Three PVT corners where simulations were performed

Corner	Temp	Process	VDD
Typical	25	TT	1.8
Slow	-40	SS	1.62
Fast	125	FF	1.98

Figures 7 and 8 show the transient responses of VDD detecting POR block and the proposed switching system.

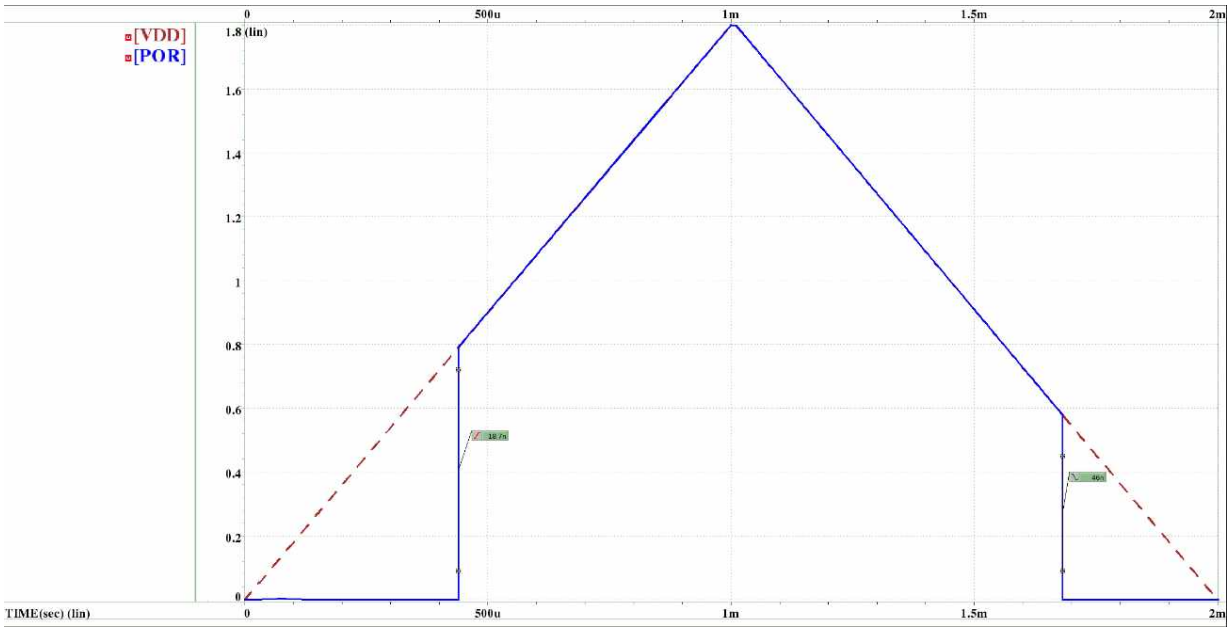

Fig. 7 Voltage detection circuit output and supply voltages

As Figure 7 shows POR block has different low-to-high and high-to-low thresholds in order to avoid false switches which would otherwise be caused by supply rail noises [3].

Figure 8 shows cases when the entirety of suggested solution is in action. In the absence of data both PADN and PADP are pulled down, VDD is off and so is ART18. When one of the data lines goes high, a voltage close to VDD is formed at the ART18 output which triggers the VDD Wake-Up block to connect other sub-circuits to power supply. When voltage at VDD node reaches around 0,8V (Typical corner) the POR output toggles on and starts shifting the supply of Wake-up logic from ART18 to VDD. When VDD reaches around 80% (1.4V for Typical corner) of its final value POR out is high enough to completely switch Wake-Up supply to VDD. The Wake-Up block, now powered by VDD, continues to monitor data lines and when they both are pulled down VDD is once again disconnected from power rail. A small delay mechanism is also added to prevent false toggle offs in case of slight data non-overlap.

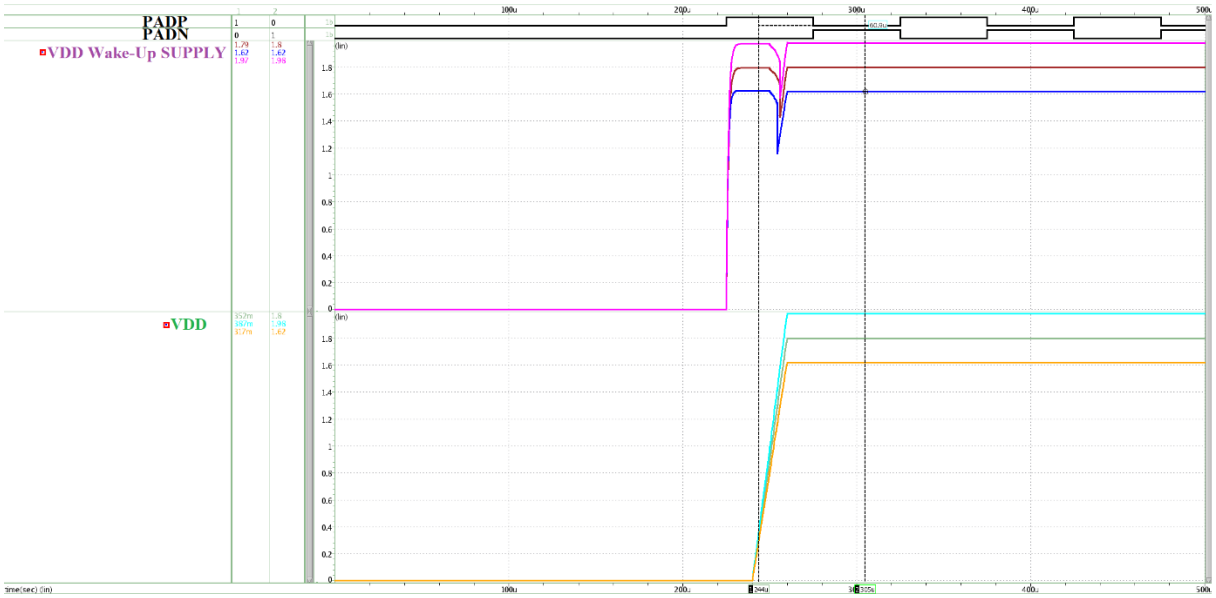

Fig. 8 Proposed supply switching architecture in action

Figure 9 shows the signal on SDL line with and without the implemented solution. In the Before signal the rising edge starts to break at around 1,.5V and the dissipating power doesn't allow the signal to reach its intended 3,3V value. After implementing the proposed solution, the signal has full 3,3V swing and the rising edge breaks at around 3V.

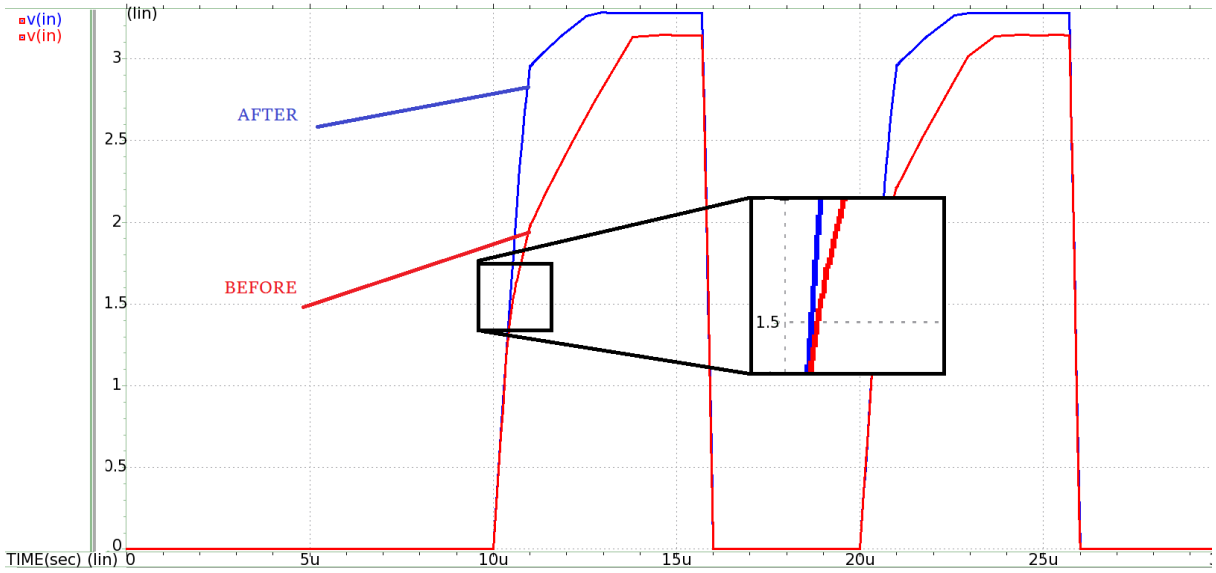

Fig. 9 Signal integrity with and without the proposed solution

Conclusion 1

A method for improving the power-efficiency of an electrical system is proposed by using data driven power supply monitoring and switching. As the power is not wasted in the absence of data, the lifetime of the system using an autonomous power source is increased. This can be very useful in systems where longevity concerns supersede startup speed requirements. Compared to other solutions the proposed architecture alleviates the need of an external stand-by control and offers a monitoring system which doesn't require a constant supply. The proposed architecture was implemented and simulated using SAED 14nm finFET technological process and HSPICE simulator. Simulation results show that the proposed architecture can provide very close to supply voltage with enough driving capacity to empower the wake-up logic circuit.

Conclusion 2

Another application of the circuit is verifying ESD events in open-drain communication interfaces thus improving the signal integrity. Simulation results show that both rising edge of the signal as well as steady state voltage are significantly closer to the ideal values with the artificial supply generator connected to the ESD protection circuit. In case of I2C protocol where rise times are measured from 30% to 70% of the steady value the added circuit twice decreases the rise time while dissipation no DC power.

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ԷՆԵՐԳԱՍՊԱՌՄԱՆ ԱՐԴՅՈՒՆԱՎԵՏՈՒԹՅԱՆ ԵՎ ԱԶԴԱՆՇԱՆԻ ԱՄԲՈՂՋԱԿԱՆՈՒԹՅԱՆ ԲԱՐԵԼԱՎՄԱՆ ՀԱՄԱՐ ՏԵՂԵԿԱՏՎԱԿԱՆ ԱԶԴԱՆՇԱՆՆԵՐԸ ԵՎ ՍՆՈՒՑՄԱՆ ԱՂԲՅՈՒՐԸ ՎԵՐԱՀՍԿՈՂ ԵՎ ՂԵԿԱՎԱՐՈՂ ՀԱՄԱԿԱՐԳ

Հ.Հ. Սահակյան, Ռ.Մ. Սողոմոնյան, Դ.Խ. Գաբրիելյան, Գ.Ա. Ոսկանյան
Հայաստանի ազգային պոլիտեխնիկական համալսարան

Էներգասպառման արդյունավետությունը և ազդանշանի ամբողջականությունն ու որակը ժամանակակից հաղորդակցման ստանդարտների նախագծման փուլի կարևորագույն

չափանիշներից են: Առաջարկվում է, էներգասպառման արդյունավետության և ազդանշանի ամբողջականության մեծացման նոր մեթոդ, որը օգտագործում է մուտքային ինֆորմացիայի հիման վրա սնուցման աղբյուրի վերահսկողության և փոպանջատման համակարգ: Ի տարբերություն ընդունված մոտեցմանը, որտեղ բազմաթիվ ծառա սարքեր գտնվելով պարապ վիճակում սպասում են ղեկավարող սարքից ազդանշանի, առաջարկվող համակարգը ներկայացնում է էներգասպառման տեսանկյունից ավելի արդյունավետ մեթոդ: Այն է՝ միացնել այս սարքերը միայն այն ժամանակ երբ նրանց տեղեկություն է փոխանցվում: Առաջարկվող համակարգը օգտվում է դիֆֆերենցիալ տեղեկության փոխանցման դողերից, որպեսզի գեներացնի կեղծ, ցածր հզորությամբ սնման աղբյուրը, որը սնում է հիմնական սնման աղբյուրի փոխանջատումները իրականացնող փոքր թվային բլոկներ: Համակարգը նաև օգտագործում է ոչ-դասական լիցքաթափում-ըստ-միացման բլոկ, որպեսզի իրականացնի սնման լարման մակարդակի վերահսկողություն: Կեղծ սնուցում գեներացնող բլոկը կարող է նաև օգտագործվել էլեկտրաստատիկ պարպման հայտնամբերման իսկությունը հաստատելով բաց-հորդան/բաց-ընդունիչ կառուցվածքով հաղորդակցման ստանդարտներում ազդանշանի որակի և ամբողջականության բարելավման համար: Շղթաները նախագծվել և նմանարկվել են օգտագործելով Սինոփսիս Արմենիա Ուսումնական Դեպարտամենտի 14նմ finFET տեխնոլոգիական գործընթացի մոդելները: Սխեմայի գրաֆիկական նախագծման և նմանարկման համար օգտագործվել են Սինոփսիս ընկերության Custom Compiler և HSPICE ծրագրային գործիքները: Տարբեր վիճակներում շղթայի աշխատանքի որակը ապահավելու նպատակով, այն փորձարկվել են 3 եզրային վիճակներում: Արդյունքում ստացած ազդանշանները ներկայացված են Custom WaveView գործիքի միջոցով:

Բանալի բառեր. ինտեգրալ սխեմաներ, էներգասպառման էֆեկտիվություն, ինֆորմացիայի բաժանիչ, էներգիայի աղբյուրի կառավարում, լիցքաթափում ըստ միացման, էլեկտրաստատիկ պարպում:

УДК - 621.382.13

СИСТЕМА МОНИТОРИНГА И КОНТРОЛЯ ИНФОРМАЦИИ И ИСТОЧНИКА ПИТАНИЯ ДЛЯ ПОВЫШЕННОЙ ЭНЕРГОЭФФЕКТИВНОСТИ И ЦЕЛОСТНОСТИ СИГНАЛА

Г.Г. Саакян, Р.М. Согомонян, Д.Х. Габриэлян, Г.А. Восканян
Национальный политехнический университет Армении

Энергоэффективность и целостность сигнала являются главными показателями в проектировании современных коммуникационных интерфейсов. Предложен новый метод для повышения энергоэффективности и целостности сигнала путём осуществления мониторинга источника энергии по входным данным, используя переключательную архитектуру. Вместо традиционного подхода, когда многочисленные устройства находятся в режиме ожидания пока не придёт сигнал от ведущего, предложенный метод предлагает более энергоэффективный подход, включая эти устройства только когда с ними связываются. Предложенная архитектура воспользуется наличием дифференциальных информационных линий в коммуникационных протоколах для генерации искусственного маломощного источника для питания малых логических блоков, которые реализуют переключение напряжений питания. Система использует нестандартный блок сброса по включению для контроля уровня питания. Блок генерации искусственного питания может быть также использован для повышения целостности сигнала в коммуникационных архитектурах открытого истока/открытого коллектора, каковыми

являются, например I2C, SCSI-1 и т.д., проверяя подлинность ЭСР в отключённых устройствах, тем самым предотвращая ненужное потребление тока. Схема была спроектирована и симулирована, используя 14нм finFET технологический процесс, разработанный Синопсис Армения Учебным Департаментом. Synopsys Custom Compiler и HSPICE были использованы для графического дизайна схемы и симулирования соответственно. Схема была протестирована в трёх крайних случаях, чтобы обеспечить стабильную работу в разных обстоятельствах. Снимки результатов были получены с помощью Custom WaveView.

Ключевые слова: интегральные схемы, энергоэфективность, делитель данных, управление источником энергии, сброс по включению, электростатический разряд.

Ներկայացվել է՝ 13.05.2020թ.
Գրախոսման է ուղարկվել՝ 15.05.2020թ.
Երաշխավորվել է տպագրության՝ 09.06.2020թ.