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THE METHOD OF IMPROVEMENT OF RELIABILITY OF OPERATIONAL AMPLIFIERS IN ANALOG INTEGRATED CIRCUITS

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Among the technical specifications set for modern integrated circuits, the parameters related to their reliability play a key role taking into account the wide sphere of applications of these circuits in areas that may be related to human life. Modeling of the aging effects of circuits at the schematic level is used as a method of reliability measurement.

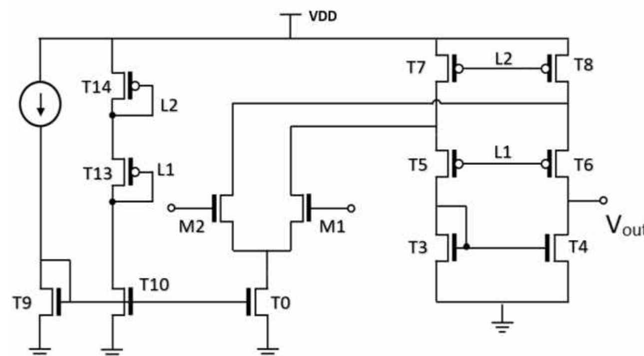
The method of improvement of reliability in analog integrated circuits is suggested where the schematic solutions provide a possibility of reduction of offset between the inputs of operational amplifiers bringing it up to 1.3mV by small increase of semiconductor surface area. The suggested method can be used in integrated circuits designed with modern 14nm and smaller technological processes.

Key words: ageing, lifetime, transistor switch, schematic modeling, threshold voltage, voltage shift.

Introduction

Integral circuits (IC) are widely used in aircrafts, vehicles, military engineering, medical equipment and elsewhere. The ICs used in such systems are of high value because compared to the ones used in household appliances, the technical requirements for both functional and reliability providing parameters are rigid [1-3].

In modern ICs analog segments which are responsible for receiving, processing and transmitting data from one IC to another, are considered to be the most sensitive ones. The key nodes of analog integrated circuits are operational amplifiers. The type of operational amplifier providing more amplification and bandwidth than many of the various architectures available is the embedded cascade operating amplifier circuit (Pic. 1) [4-5]. The high value of the amplification factor is due to the multi-cascade structure and the great bandwidth is a result of the embedded cascading architecture without Miller's phenomenon. Meanwhile, as a result of the application of such architecture, the input working range of the operational amplifier increases which makes it possible to amplify the analog signal with a larger amplitude without distorting its appearance. On the other hand, with 3 output cascades the probability of transistors leaving the saturation mode is minimized [6-8]. Considering the above mentioned fact, further research has been done on this architecture with the aim of improving its reliability and ensuring 10 years of uninterrupted operation.



Picture 1 The current circuit of operational amplifier

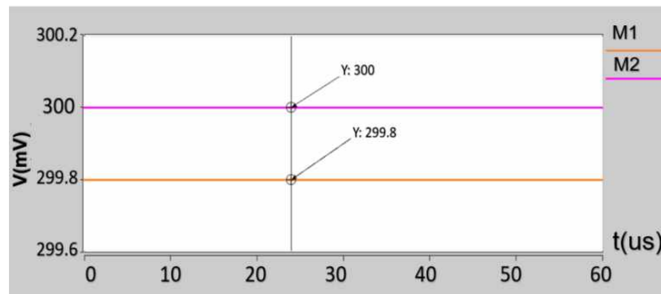
A number of reliability parameters are used in the designing process of the modern integral circuits. These include electromagnetism, verification of the possibility of exceeding the maximum permissible voltage of the transistor nodes and testing the aging of individual IC transistors etc [9-12]. The work is dedicated to the improvement of the key parameters of the operational amplifiers which are part of analog integral circuits because of aging. The aging is estimated according to the working years of the IC, though it is clear that it's impossible to wait, for instance, 10 years to detect problems available in the IC nodes. Therefore, schematic modeling is done for the implementation of the latter using special aging models of transistors [13-14]. There are well-known mathematical formulas that describe the aging process and the main influencing factors. The mathematical formula for the shift in the threshold voltage of the transistor as a result of such aging is presented below [15]:

$$\Delta V_{TH} \sim C_{HC}\frac{1}{\sqrt{L}}\exp(\propto_1 E_{one})\exp(\propto_2 V_{DS})\, t^{n_{HC}}$$

wherein n_{HC} is the time exponent, E_{one} is the electric field applied to the valve insulator, C_{HC} is a constant value describing the technological process, L is the length of the transistor channel, V_{DS} is the voltage applied between the drain and source of the transistor, $\propto_1$ and $\propto_2$ are the voltage scale coils.

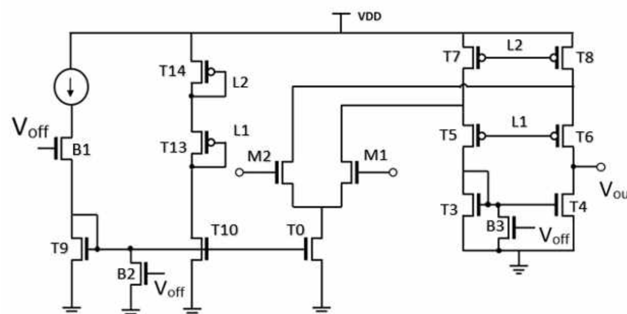
Conflict setting

In order to clarify the phenomenon of aging, to identify the main influencing factors and to mitigate their effects, the scheme of the operational amplifier with the embedded cascade is considered in two modes – power on and power off. In the operating mode any significant aging or deviation of the functional parameter are not recorded (Pic. 2).



Picture 2 The results of modeling the operational amplifier after being aged in 10 years of operating mode

After simulating the aging of the circuit in the power off mode and applying it in the negative feedback loop, the measurements showed that there is a voltage deviation between the positive and negative inputs of the amplifier. The disconnected mode of the circuit is provided by B1, B2 and B3 N-type metal-oxide-semiconductor (NMOS) transistors (Pic. 3).



Picture 3 The circuit of the operational amplifier providing the switching mode with transistor switches

At the gates of the transistors specified in the off mode, a logical “1” signal is applied, opening them and equalizing the potentials of the corresponding nodes to zero. One of the main reasons for aging is that in the current circuit with availability of power supply high-impedance nodes are formed and in the case of a 10-year aging model their threshold voltage shifts. Depending on the type of design, in the power off mode case, signals with the following combinations may be applied to the input M1 and M2 transistor gates:

1) M1 - ´0´ and M2 - ´0´
2) M1 - ´0´ and M2 - ´1´
3) M1 - ´1´ and M2 - ´0´
4) M1 - ´1´ and M2 - ´1´

wherein the logical ‘‘0’’ level is equal to 0V and ‘‘1’’ is equal to the value of the supply voltage.

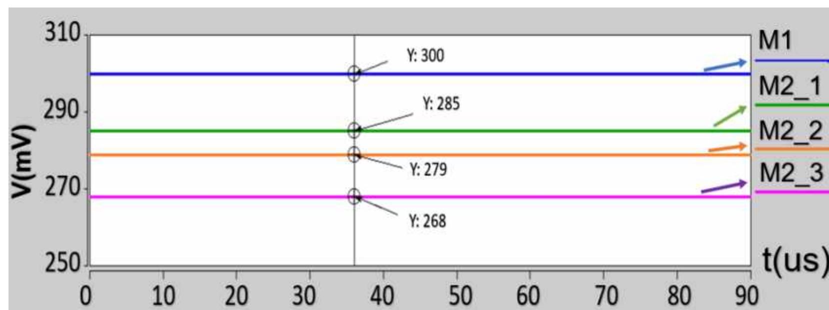
The threshold voltage shifts of input transistors caused by the aging are presented in the Table 1.

Table 1

The shifts in the threshold voltage of the current circuit’s input transistors caused by aging after 10 years of operation

Combination of input signals	M1 transistor’s threshold voltage shift (mV)	M2 transistor’s threshold voltage shift (mV)
M1 - ´0´ and M2 - ´0´	56	56
M1 - ´1´ and M2 - ´1´	260	260
M1 - ´1´ and M2 - ´0´	258	55
M1 - ´0´ and M2 - ´1´	55	258

The maximum change in the threshold of transistors voltage is recorded when the transistors are in the open state. The modeling to assess the effect of a threshold voltage shift on the parameters of operating amplifier in the operating mode of the circuit has shown offset of up to 32 mV between its inputs (Pic.4).



Picture 4 The voltage deviation in the off mode between the input transistors in the operational amplifier

Table 2 shows the offset between the inputs of operational amplifier in the power off mode depending on the signals applied to the inputs as a result of 10 years of aging.

Table 2

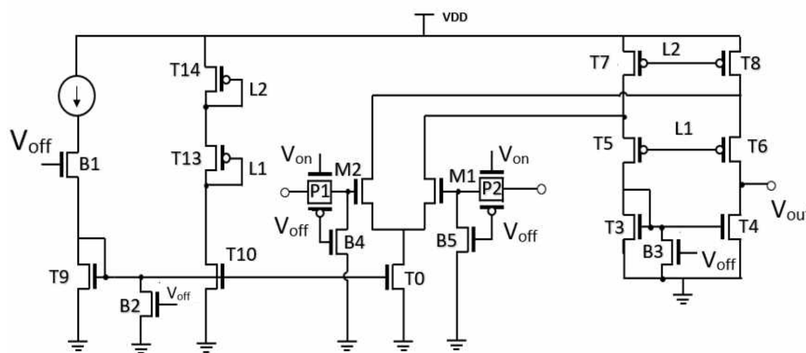
The results of the voltage deviation recorded in the inputs of the operating amplifier after staying in the power off mode for 10 years

Combination of input signals	Offset (mV)
M1 - ´0´ and M2 - ´0´/ M2_1	15
M1 - ´1´ and M2 - ´1´/ M2_2	21
M1 - ´1´ and M2 - ´0´/ M2_3	32

Combining the results of Table 1 and Table 2 we can conclude that on the one hand, the threshold voltages of the transistors are mostly shifted when they are open, and on the other hand, the reason for the deviation between the inputs of the operational amplifier is the reverse deviated input transistors. The task is to decrease the offset between the inputs of the operational amplifiers by using schematic solutions thus increasing their reliability and ensuring 10 years of uninterrupted operation.

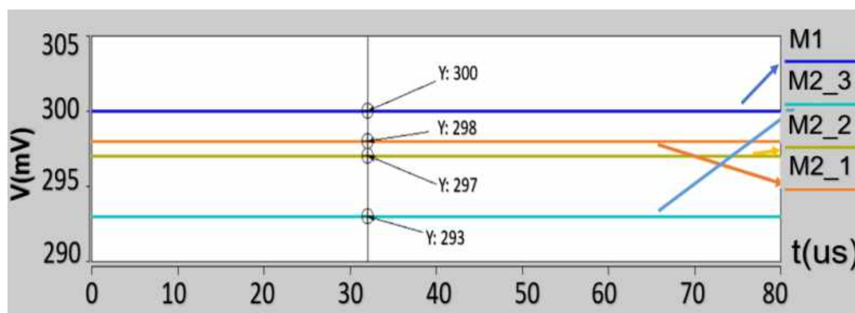
Research results

Multiple researches to solve this problem have shown that in order to reduce threshold voltages as well as to reduce offset between the inputs of the operational amplifier, it is necessary to make such schematic changes that the input N-MOS transistors should be closed or deviated to the same side. In order to implement the latter, the inputs of the operational amplifier are isolated from the primary inputs of the circuit by means of the switches combined with N and P transistors. At the same time, the B4 և B5 switches are added, resulting in the closure of the input M1 and M2 transistors in the circuit power off mode (Pic. 5).



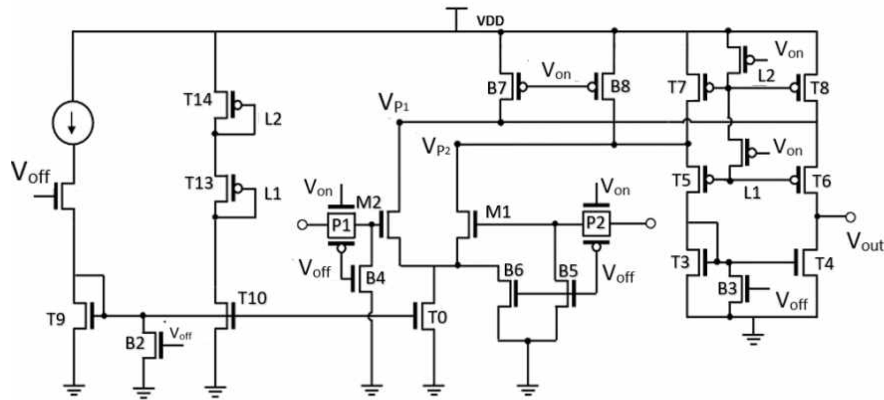
Picture 5 The suggested circuit of the operational amplifier with the application of B4 and B5 switches

The results of the schematic modeling to evaluate the effectiveness of the proposed solution showed a significant improvement in the detected problems, in particular, the offset between inputs of the operational amplifier has decreased from 32 mV to 7 mV.



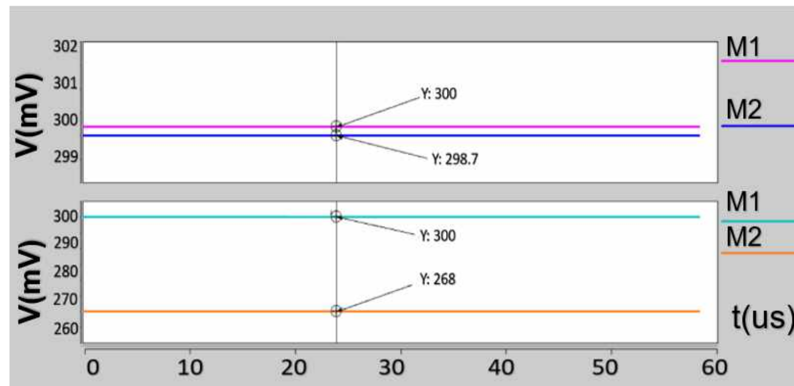
Picture 6 The offset voltage of the operational amplifier with the presence of B4 and B5 switches

However, this index of improvement is not enough as it is comparable to the levels of signals developed in modern analog ICs. In order to further improve the obtained results, all the secondary nodes of the circuit which can be in high impedance and cause such problems have been considered. To solve this problem, transistor switches have been added to the L1, L2, Vp1 and Vp2 nodes which connect them to the power supply in the power off mode of the circuit (Pic. 7).



Picture 7 The suggested circuit of the operational amplifier

In the proposed circuit in contrast to the existing one, there are no high-impedance nodes, there is no possibility of a reverse deviated voltage across the inputs. The results of the schematic modeling prove the effectiveness of the method (Pic. 8) - the maximum offset between the inputs of the operational amplifier does not exceed 1.3 mV.



Picture 8 The offset of input voltage as a result of 10 years of aging in a power off mode using the proposed and current method of operational amplifier

The obtained results are summarized in Table 3.

Table 3

The research results of the operational amplifier designed with using the proposed method

Parameter	Available circuit	Proposed circuit
Maximum input voltage offset (*mV*)	32	1.3
Maximum shifting of transistor’s threshold voltage	260	40
Power consumption (uW)	100	100
Surface occupied by semiconductor crystal (um^2)	167	172

Conclusion

SAED14nm FinFet technological process has been implemented in the design of the operational amplifier with an embedded cascade. As a result of the proposed schematic-technical solutions, it is possible to increase the reliability of the amplifier by changing the 32 mV offset of 10 years aging between the inputs to 1,3 mV. The proposed solutions do not lead to an increase in the power consumption of the circuit and the surface occupied by the semiconductor crystal increases slightly by 5 um^2, which is only 3% of the surface occupied by the operational amplifier.

We can conclude that if the designed IC is used approximately 10 years, this method will give an opportunity to have reliable parameters of operational amplifiers.

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ԱՆԱԼՈԳԱՅԻՆ ԻՆՏԵԳՐԱԼ ՍԽԵՄԱՆԵՐՈՒՄ ՕՊԵՐԱՑԻՈՆ ՈՒԺԵՂԱՐԱՐՆԵՐԻ ՀՈՒՍԱԼԻՈՒԹՅԱՆ ԲԱՐՁՐԱՑՄԱՆ ՄԵԹՈԴ

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Ժամանակակից ինտեգրալ սխեմաներին առաջադրվող տեխնիկական առաջադրանքների մեջ առանցքային տեղ են գրավում դրանց հուսալիությանը վերաբերող պարամետրերը՝ հաշվի առնելով այդ սխեմաների լայն կիրառությունը այնպիսի բնագավառներում, որոնք կարող են առնչվել մարդկային կյանքերի հետ: Որպես հուսալիության չափման եղանակ կիրառվում է սխեմաների ծերացման երևույթի մոդելավորումը սխեմատեխնիկական մակարդակում:

Առաջարկվում է ծերացան հետևանքով անալոգային ինտեգրալ սխեմաներում հոսալիության անկման բարելավման մեթոդ, որտեղ սխեմատեխնիկական լուծումների ներդրման արդյունքում հնարավորություն է ստեղծվում փոքրացնելու օպերացիոն ուժեղարարների մուտքերի միջև առաջացող լարման շեղման չափը՝ հասցնելով այն ընդհուպ 1.3մՎ-ի՝ ի հաշիվ այդ սխեմայի՝ կիսահաղորդչային բյուրեղի վրա զբաղեցրած մակերեսի չնչին ավելացման: Առաջարկվող մեթոդը կարող է կիրառվել ժամանակակից 14նմ և ավելի փոքր տեխնոլոգիական գործընթացներով նախագծվող ինտեգրալ սխեմաներում:

Բանալի բառեր. ծերացում, կյանքի տևողություն, տրանզիստորային բանալի, սխեմատեխնիկական մոդելավորում, շեմային լարում, լարման շեղում:

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МЕТОД УВЕЛИЧЕНИЯ НАДЕЖНОСТИ ОПЕРАЦИОННЫХ УСИЛИТЕЛЕЙ В АНАЛОГОВЫХ ИНТЕГРАЛЬНЫХ СХЕМАХ

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В технических заданиях на проектирование современных интегральных схем, учитывая широкое использование данных схем в отраслях тесно связанных с жизнедеятельностью человека, ключевое место отводится параметрам характеризующим надежность. В качестве метода оценки степени надежности используется моделирование процесса старения схемы на схемотехническом уровне.

В данной статье предлагается метод уменьшения степени деградации надежности аналоговых интегральных схем, возникающей в процессе старения. Данный метод, в результате использования ряда схемотехнических решений позволяет, уменьшить разность напряжений возникающую между входами операционных усилителей, доводя таким образом значения разности до 1.3мВ, за счет незначительного увеличения площади занимаемой данной схемой на полупроводниковом кристалле. Предлагаемый метод может быть использован при проектировании интегральных схем по технологическим процессам 14нм и меньше.

Ключевые слова: старение, ожидаемый срок службы, транзисторный переключатель, схематическое моделирование, пороговое напряжение, отклонение напряжения.

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