UDC - 621.375.132

THE METHOD OF IMPEDANCE OF RECEIVER/TRANSMITTER CALIBRATION IN INTEGRATED CIRCUITS WITH ANALOG SUBTRACTOR

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Complementary metal-oxide-semiconductor (CMOS) technology is constantly being modernized as a result of which the minimum size of transistors is being scaled. Year by year modernizing technology has led to an increase in the number of transistors placed on the same surface. As a result the specifications on the performance of the circuits have become more complex.

Due to the low cost and high performance, the CMOS receiver and transmitter circuits sequentially have been widely used in modern applications. One of the main problems in the transmitter-receiver circuits is correspondingly their output and input impedance calibration. The method of resistance calibration is proposed which is based on the analog subtractor.

The use of the method allows to significantly reduce the calibration time by a small required increase of surface area.

Key words: Coordination, external resistance, reflection coefficient, long lines, characteristic impedance, logic module.

Introduction

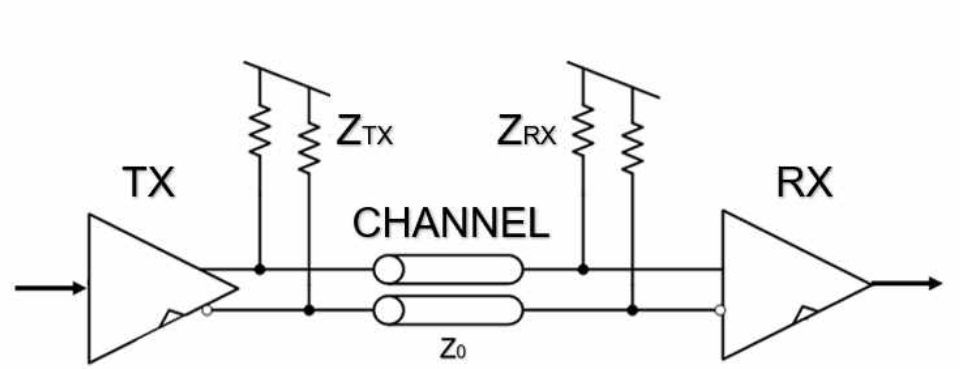
The rapid development of the production of technologies of integrated circuits (IC) as well as its combination with innovative architectural solutions have led to the engineering of highly efficient digital systems [1]. Along with the growth of the high-speed industry, new problems have arisen that cannot be solved by implementing previously applied solutions. One of these problems is the phenomenon of distortion during the transmission of a high-frequency signal from one system to another. Therefore, to transfer data without any loss, firstly it is necessary to ensure a stable connection between several integrated circuits. For this very purpose, high-speed transmitter-receiver circuits have been developed [2]. One of the main limiting factors of the high-speed performance is the reflection of the signals transmitted at the input/output circuits which emerge due to the incompatibility of the output line of the transmitter and the input impedances of receiver. The transmitting data is either not obtained by the receiver on the transmission line or it reaches with a low amplitude which often does not allow the transmitter to accurately recover the transmitted data [3]. In order to avoid or minimize the reflections during the data transmission, it is necessary to adjust the impedance of input/output circuit. However, in order to ensure high accuracy, the adjustment process often becomes time-consuming and affects the high-speed performance of the system negatively [4].

This research aims at designing a circuit for calibrating the input and output impedances of the transmitter the calibration time of which will be less than that of the current solutions.

Conflict setting

The technical requirements for the modern integrated circuits are strict. It is necessary to design such circuits that will be able to work accurately in the changing conditions of ±10% of power supply voltage and -40..150℃ of ambient temperature taking into consideration also the deviations of the parameters of capacitors, resistors and transistors caused by the imperfection of the technical process.

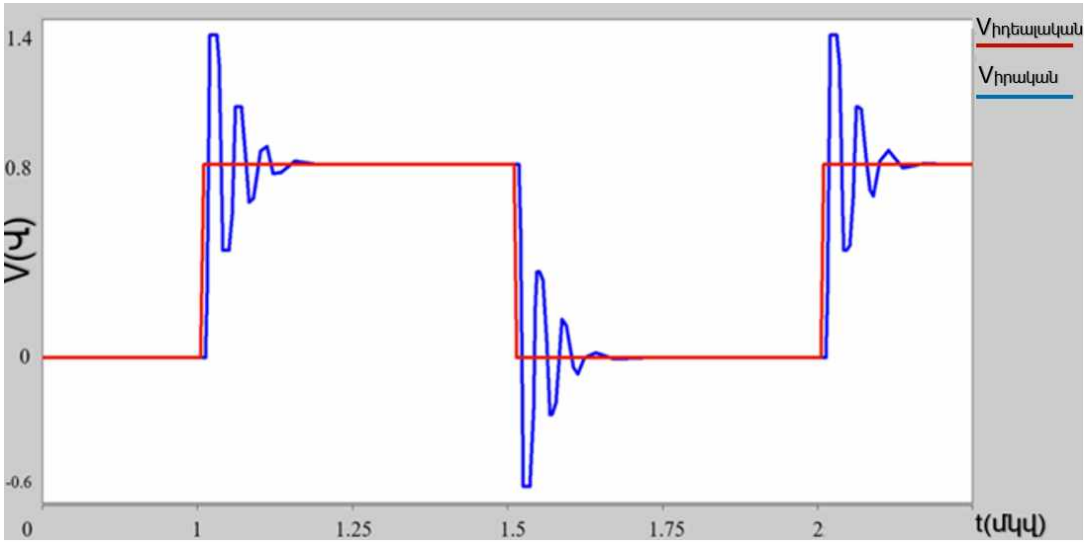
Keeping in mind the above mentioned fact, the system of impedance calibration must ensure high stability for all these factors.



Picture 1 The simplest circuit of the transmitter-receiver system

When the resistances z_{TX}, z_0 and z_{RX} are not coordinated, signal reflections occur and the only way to avoid this is to minimize the speed of the transmitted data (pic. 2), which affects the high-speed performance of the developed system negatively. In order to avoid reflections, the transmitter and receiver reflection coefficients must be zero.

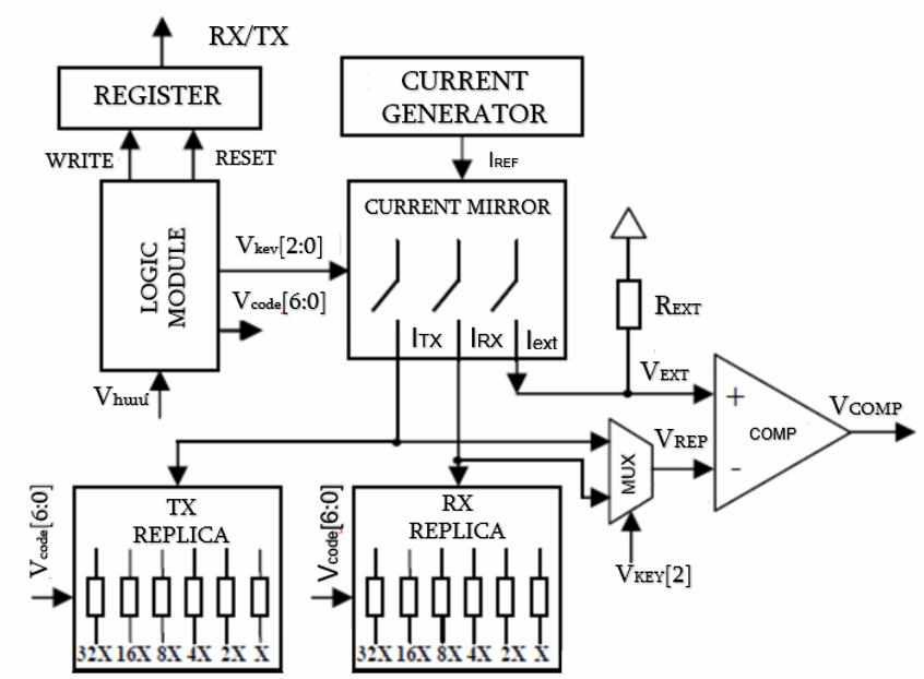
$$\rho_{CH} = \frac{z_{TX} - z_O}{z_{TX} + z_O} \qquad \rho_{CH} = \frac{z_{RX} - z_O}{z_{RX} + z_O} \tag{1}$$



Picture 2 The results of the ideal signal distortion caused by reflections

(1) implies that the reflection coefficients will be equal to zero when the z_0, $z_{receiver}$ և $z_{transmitter}$ impedances will be equal to each other.

After some time of the working mode of existing circuit the logic module generates 7 bit signals which extends to the 7 switches in the replica block [5]. The I_{ext} current flows through an external resistor with 200 Ω creating V_{ext} voltage drop. The logic module changes the code going to the replica block from 0 to 63. As the code grows, the number of resistors connected parallelly in the replica block increases thus reducing the value of the settling impedance. The I_{REF} current flows through the resistance of the replica block creating V_{rep} voltage drop.



Picture 3 The existing circuit of the calibration system

The positive input of the comparator is connected to V_{ext} and the negative one to V_{rep}. As the code grows the drop of V_{rep} voltage is decreasing. When V_{rep} gains smaller value than V_{ext} the output of the comparator is switched from "0" to "1""and the logic module records the corresponding code in the digital register. In this case of solution to ensure high accuracy, the bit value of the calibration impedance circuit is increased as a result of which the time required for the calibration and the surface occupied by the semiconductor crystal are increased.

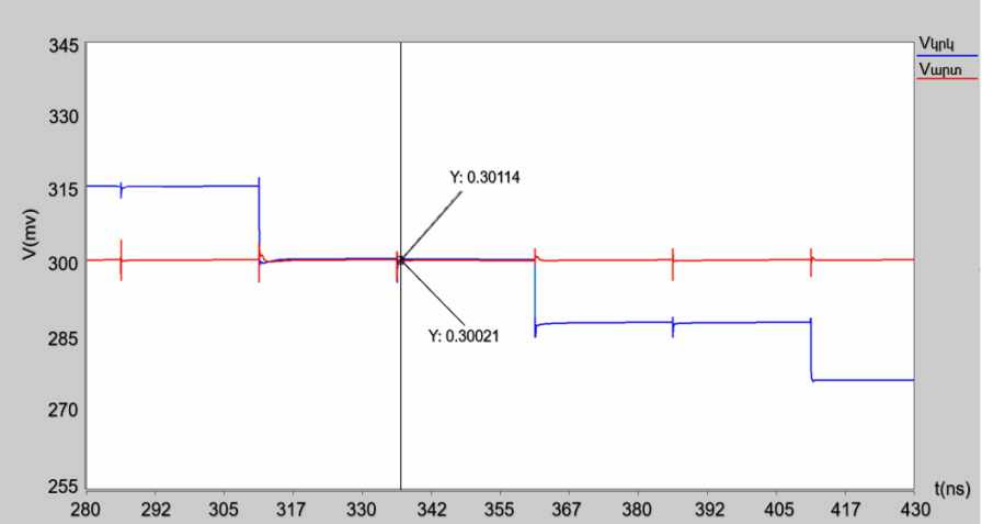
In order to improve the efficiency of the calibration process, it is proposed to develop a new method that will again provide high adjustment efficiency, but will require lower bit value, less adjustment time and will be designed with the modern 14nm FinFet technology.

The method of impedance calibration with analog subtractor

In the considered method, the change in the voltage drop across the replica resistor from the largest value to the smallest is carried out by 63 steps as a result of which 6 values are used for the calibration.

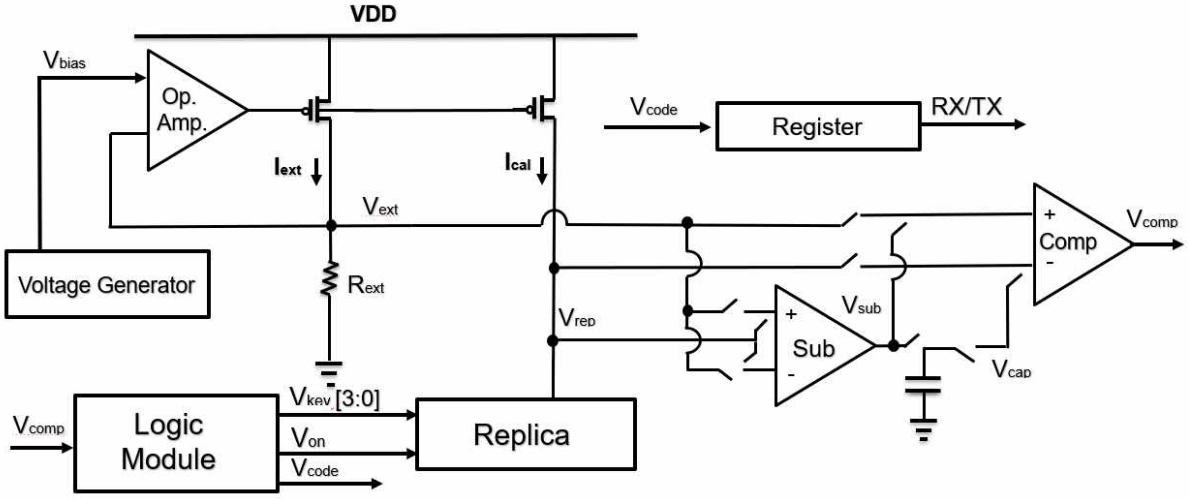
$$N_{step} = 2^n - 1 \quad (2)$$

In order to increase the high-speed performance, it is suggested to reduce the bit value of the generated code up to 4. As a result of applying the proposed method, a larger voltage shift over the resistance in the replica block is expected at each step than in the existing system. The schematic modeling shows (Pic. 4) that the mutual alignment between V_{ext} and V_{rep} voltages has been changed. At the 310-360ns time range V_{rep} is still higher than the V_{ext}, but the voltage difference is about 1 mV. According to the current method, the code should be selected corresponding to the 360-410 time domain, as in that case the output of the comparator is shifted from "0" to "1".



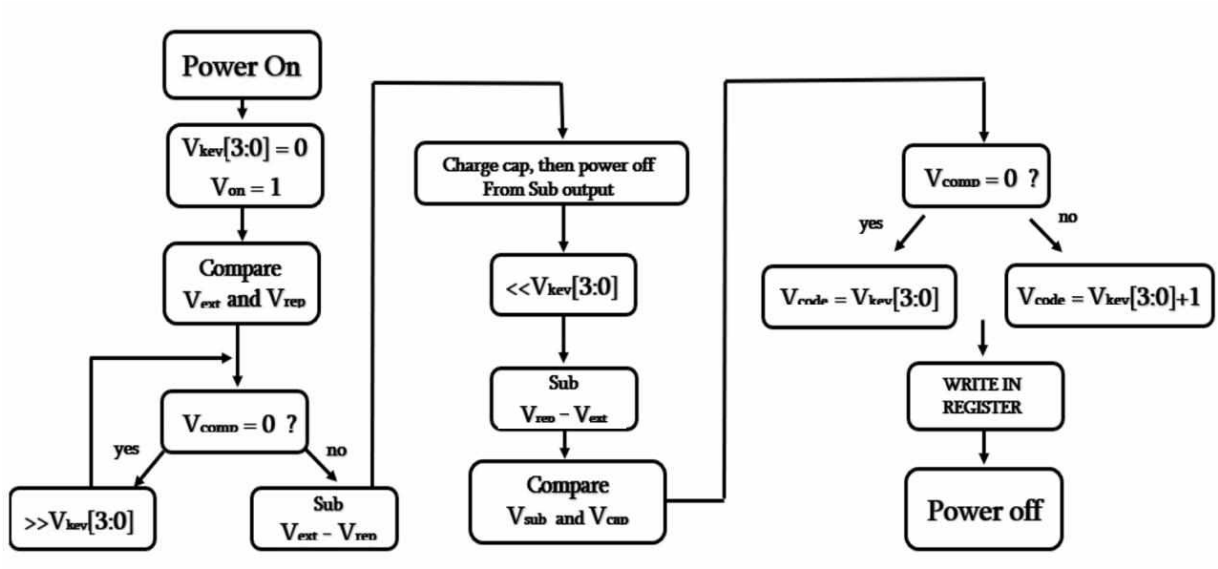
Picture 4. The results of V_{ext} and V_{rep} modelling

In order to get a more accurate resistance, it is necessary to choose the previous code according to the results of the modeling. In order to implement the latter, a new method is proposed where the analog subtractor circuit has been utilized. With the help of the analog subtractor, the system has the opportunity to distinguish which of the following codes is preferable. The code at which the difference between V_{ext} and V_{rep} voltages will be the minimal will be considered preferable and as a result a more accurate resistance value will be gained.



Picture 5 The proposed circuit of impedance calibration with analog subtractor

The reduction of the calibration time is conditioned by the demotion of the generated code range and the improvement of the logic module. In the case of the proposed logic module there is no need to increase the code to the maximum value. When the comparator output records '0' – '1' exchange, the further growth of the code stops and instead several actions are implemented which are described in the algorithm (Pic. 6).



Picture 6 The proposed digital system designing of impedance calibration

Research results

The results of the research are summarized in Table 1. We see from the table that when applying the proposed method, the calibration time has been reduced by approximately 3 times. Such a significant reduction is possible due to the fact that the system no longer spends time on the further growth of the code finding the required code. The simulation is implemented in more technological deviation cases and in larger scale of temperature change.

The proposed circuit is simulated with the SAED14nm FinFet technology process. The simulation has been carried out with the help of HSIPCE schematic modeling tool of Synopsys. The results have been displayed with the CosmosScope software tool.

Table 1

The summary of results

Parameter	Current circuit	Proposed circuit
Maximum resistance deviation (%)	2.1	1.3
Calibration period (*us*)	3.2	1.05
Power consumption (*mW*)	12.4	8.2
Temperature conditions (^{0}C)	55, 125, -40	25, 150, -40
Technical process	TT, SS, FF	TT, SS, FF, SF, FS

Conclusion

The use of an analog subtractor in the calibration circuit as well as the improvement of the digital system designing algorithm has provided an opportunity to increase the calibration accuracy by more than 1,6 times. At the same time the calibration period has been reduced more than 3 times and the power consumption has been decreased by 1,5 times. The circuit has been designed with the modern 14nm FinFet technical process and can be utilized in the receiver-transmitter circuits currently being designed.

Therefore, whenever it is necessary to have less calibration time and opportunity to increase the design surface with a small amount, the proposed method is a good solution.

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ՀՏԴ - 621.375.132

ԻՆՏԵԳՐԱԼ ՍԽԵՄԱՆԵՐԻ ԸՆԴՈՒՆԻՉ ՀԱՂՈՐԴԻՉ ՀԱՆԳՈՒՅՑՆԵՐՈՒՄ ԱՆԱԼՈԳԱՅԻՆ ՀԱՆԻՉԻ ԿԻՐԱՌՄԱՄԲ ԴԻՄԱԴՐՈՒԹՅՈՒՆՆԵՐԻ ԿԱՐԳԱԲԵՐՄԱՆ ՄԵԹՈԴ

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Կոմպլեմենտար մետաղ-օքսիդ-կիսահաղորդիչ (ԿՄՕԿ) տեխնոլոգիան ենթարկվում է անընդհատ արդիականացման, որի արդյունքում տեղի է ունենում տրանզիստորների նվազագույն չափերի մասշտաբավորում: Տարեցտարի արդիականացող տեխնոլոգիան բերում է նրան, որ միևնույն մակերեսի վրա տեղակայված տրանզիստորների քանակը ավելանում է: Արդյունքում խստանում են նաև սխեմաների արագագործությանն առաջադրվող սահմանափակումները:

Ցածր ինքնարժեքի և բարձր թողունակության շնորհիվ ԿՄՕԿ հաջորդական կապով ընդունող և հաղորդող հանգույցները մեծ կիրառություն են գտել ժամանակակից սարքավորումներում: Հաղորդիչ-ընդունիչ հանգույցներում կարևոր խնդիրներից մեկը հաղորդչի ելքային, փոխանցման գծի և ընդունիչի մուտքային դիմադրությունների համաձայնեցումն է:

Առաջարկվում է մեթոդ, որի կիրառմամբ իրականացվում է ընդունիչ-հաղորդիչ հանգույցների դիմադրությունների կարգաբերում՝ ի հաշիվ անալոգային հանիչի ներդրման:

Մեթոդի կիրառումը թույլ է տալիս զգալիորեն կրճատել կարգաբերման ժամանակը մակերեսի ոչ զգալի մեծացման հաշվին:

Բանալի բառեր. Համաձայնեցում, արտաքին դիմադրություն, անդրադարձման գործակից, երկար գծեր, ալիքային դիմադրություն, տրամաբանական մոդուլ:

УДК - 621.375.132

МЕТОД РЕГУЛИРОВКИ СОПРОТИВЛЕНИЯ В УЗЛАХ ПРИЕМА И ПЕРЕДАЧИ ИНТЕГРАЛЬНИХ СХЕМ С ПОМОЩЬЮ АНАЛОГОВОГО ВЫЧИТАТЕЛЯ

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Технология производства комплементарной металл-оксид-полупроводниковой (КМОП) техники постоянно совершенствуется в результате чего происходит масштабирование наименьших размеров транзисторов. Из года в год развитие технологии приводит к увеличению количества транзисторов на единице площади. В результате чего также ужесточаются требования к быстродействию схем.

Благодаря низкой себестоимости и высокой пропускной способности узлы приема и передачи с последовательным соединением КМОП находят широкое применение в современных устройствах. Одной из важнейших задач в узлах приема и передачи является согласование входных сопротивлений с выходной линией передачи. В предлагаемом методе осуществляется регулировка сопротивлений узлов приема и передачи с применением аналогового вычитателя.

Применение данного метода позволяет значительно сократить время регулировки за счет незначительного увеличения площади.

Ключевые слова: координация, внешнее сопротивление, коэффициент отражения, длинные линии, волновое сопротивление, логический модуль.

Ներկայացվել է՝ 15.05.2020թ.
Գրախոսման է ուղարկվել՝ 15.05.2020թ.
Երաշխավորվել է տպագրության՝ 19.06.2020թ.